The Hong Kong Community College
CCN2272 Logic Design – Assignment 2 (Part B)

Submission deadline: ~~30 Nov 2018, 6:00pm~~ (Extended to 6 Dec 2018, 6:00pm)

Name: _____ Student Number: _____

Expected Learning Outcomes

- Explain the fundamental principles of digital logic systems and microprocessor systems.
- Analyse and design simple combinational and sequential logic systems.
- Describe the principles and applications of programmable logic devices.
- Recognise the basic structure, organisation and assembly language programming techniques of microprocessor systems.

Instructions:

1. Answer **ALL** questions. Put your answers in the space provided in the question paper. Show your steps clearly in your calculation.
2. Submit your hard copy to the pigeon hole box number 004 (15/F, HHB campus) before the deadline.

Marks of Assignment Two

Part A (30%)	

Part B

Q1 (25%)	
Q2 (25%)	
Q3 (20%)	
Total:	

Question 1 (25%)

The two-dimensional state table of a Mealy sequential circuit is given below.

Present state	Next state		Output Z	
	Input W = 0	Input W = 1	Input W = 0	Input W = 1
A	C	A	0	1
B	A	B	1	0
C	B	D	1	0
D	X	B	Y	0

State X can be one of the following states: A, B, C or D, which is derived with the 5th digit of your student ID number. Value Y can be either 1 or 0, which is derived with the 6th digit of your student ID number.

X and Y	**Determined by**
X	$a = p \ mod\ 4$, where p is the 5th digit of your SID number
Y	$Y = q \ mod\ 2$, where q is the 6th digit of your SID number

For finding **X**:

Value of *a*	**X is**
0	A
1	B
2	C
3	D

Example: if your student identity number is 1734**25**98A, then,

a = 2 mod 4 = 2, X is **C**. Y = 5 mod 2 = **1**.

(a) Derive X and Y of your sequential circuit.

(b) Draw the state diagram for the circuit.

(c) Assign the states in the circuit using counting order. Hence, construct the state table for the circuit again using state variables *A* and *B*.

(d) Implement the sequential circuit based on your result in (c), using T flip-flops and logic gates.

Answers for Q1 Marks: / 25

Question 2 (25%)

This question concerns a synchronous sequential counter, which counts an arbitrary sequence. The properties of the counter include the following:

1. The counter has one input, CLK (Clock), and three outputs, A, B and C. A is the most significant digit in the counting value, and C is the least significant digit.
2. The counter counts under a POSITIVE clock edge. It counts the numbers 1 to 7 (i.e., 001 to 111 in binary) in an arbitrary sequence. The counting sequence is:

   1, **X**, **Y**, **Z**, 3, 2, 7, 1, …

   Values of X, Y, Z can be 4, 5, 6, depending on the 4^{th} to 6^{th} digits of your student identity number and according to the rules below:

   i. Assign a "position digit", which ranges from 4 to 6, to each of the 4^{th} to 6^{th} digits of your student identity (SID) number. 4 is assigned to the 4^{th} digit, 5 is assigned to the 5^{th} digit, and 6 is assigned to the 6^{th} digit.
   ii. Based on the magnitude of the SID digits, rearrange the position digits so that the first one refers to the smallest among 4^{th} to 6^{th} digits, the second one refers to the second smallest among 4^{th} to 6^{th} digits, and the last one refers to the largest among 4^{th} to 6^{th} digits.
   iii. The counting sequence X, Y, Z is the rearranged sequence of the position digit.
   iv. If two or more digits from 4^{th} to 6^{th} digits are equal, the digit at smaller position is considered smaller.

   (Example: if your student identity number is 175822 58A, the counting sequence is 1, **5, 6, 4**, 3, 2, 7, 1, **5, 6**, ……) (Note: 5^{th} and 6^{th} digits are the same, consider 5^{th} digit being smaller.)

(a) Write down the counting sequence of your counter, starting from 1 until it returns to 1.

(b) Write down the state table of your counter. You can assume that the states that do not occur are don't care conditions.

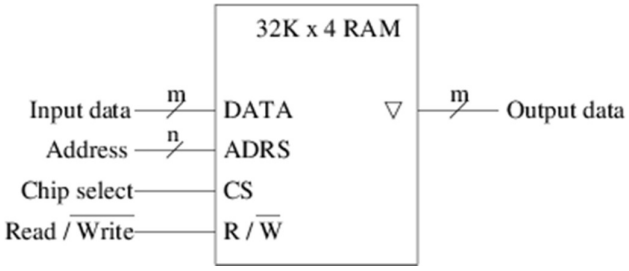
(c) Design the counter using positive-edged triggered JK flip-flops. Show your design steps clearly in your work. As the final result, draw the logic circuit diagram of your counter.

(d) Draw the output waveforms of your counter, as the clock signal is applied to the flip-flops. In your diagram, you need to include both the clock input and counting outputs waveforms. Draw the waveforms for count values starting from 1 until the counter returns to 1.

Answers for Q2 Marks: / 25

Question 3 (20%)

Consider the 32K × 4 RAM chip in the figure below.



(a) What is the size of memory (in bytes) provided by one 32K × 4 RAM chip?

(b) Suggest the values of *m* and *n* in the figure above.

(c) Assume that the 32K × 4 RAM chip uses coincident decoding to select one RAM cell, where a 9-to-512-line decoder is used as the row decoder. What is the size of the column decoder in the RAM chip?

(d) Suppose a memory, which has 16 bits per word and a capacity of 512 Kbytes, is constructed by a number of 32K × 4 RAM chips above.

(i) How many RAM chips are needed to construct such memory?

(ii) How many address lines are required to access such memory?

(iii) Following part (ii) above, describe where each part of the memory address goes to inside the memory structure, in order to access data in a RAM chip.

(iv) How many RAM chips in the memory will be selected (i.e., its chip select input is 1) when a word is being accessed?

(e) You are asked to implement **THREE** of the four microoperations as described in the following RTL statements between two 4-bit registers $R1$ and $R2$.

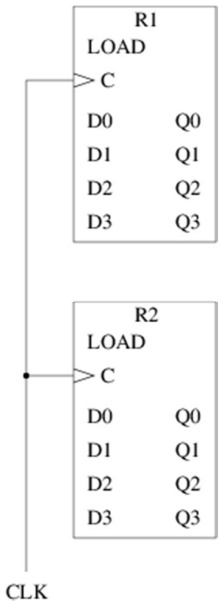
Miccrooperations	RTL
A	$R2 \leftarrow R1 \wedge \overline{R2}$
B	$R2 \leftarrow 1$
C	$R2 \leftarrow R1 \oplus R2$
D	$R2 \leftarrow \overline{R1} \vee R2$

Based on the table below, determine which **THREE** microoperations are considered in your question, and which microoperation is controlled by the control variables $C0$, $C1$ and $C2$.

Result of *a mod 3*, where *a* is 8th digit of SID	**Microoperation controlled by which control variables**		
	$C0$	$C1$	$C2$
0	A	B	C
1	C	D	B
2	D	B	A

Assume that the control variables $C0$, $C1$ and $C2$ are mutual exclusive (i.e., only one variable can be equal to 1 at any time). Also, if all control variables are equal to 0, no transfer to $R2$ should take place.

Use the Figure below to draw the logic circuit diagram of the implementation using two 4-bit registers $R1$ and $R2$, and AND gates, OR gates, XOR gates and inverters. You are **NOT** allowed to use multiplexers in your design. For simplicity, you only need to draw the connections for a single bit of register transfer operation.



Answers for Q3 Marks: / 20

(e)